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Ultra-Low Power Hybrid PLL Frequency Synthesizer with Lock Check Provisioning Efficient Phase Noise

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An accurate frequency synthesizer is essential in wireless communications, radar systems, and frequency metrology. However, open-loop signal sources exhibit severe frequency fluctuation and are vulnerable to supply-induced frequency drift, phase noise, power consumption. There is a demand for precise oscillation frequency with wide tuning range and low phase noise. This motivates the proposed synthesizer to achieve relatively lower in-band phase noise as well as good out-of-band phase noise through the use of digital amplitude control circuit. This paper presents a low power, low phase noise, and fast locking CMOS PLL frequency synthesizer. The frequency synthesizer is designed by using the 65nmCMOS technology. It can support LTE, GSM/EDGE application with the frequency ranged from 4.39 GHz to 5.71 GHz for the local oscillator in the RF front-end circuits. This paper achieves the faster locking with the lock check through controlling the phase detector and charge pump to enhance the locking speed of the proposed PLL. By implementing the proposed design, the locking speed can be enhanced along with minimum power consumption and phase noise.

Keywords: hybrid PLL, frequency synthesizer, amplitude control circuit, lock check, GSM/EDGE and LTE

1. INTRODUCTION

With the increasing demand for higher data rates and more reliable service capabilities for wireless devices, wireless communication systems suggest that millimeter-wave frequencies are very promising for future wireless communication networks due to the massive amount of raw bandwidth and potential multi gigabit-per-second (Gb/s) data rates [1]. In high-speed communication, Design with standard digital technologies phase locked loop (PLL) has been considered to relax the tight requirements of operating frequency of oscillator [2]. A PLL is a closed-loop feedback control system, which synchronizes its output signal in frequency, as well as in phase, with an input signal [3]. Commonly all PLL techniques are composed of three building blocks 1) phase detector (PD), 2) loop filter (LF) and 3) voltage-controlled oscillator (VCO). The main difference among different PLLs typically lies in how the PD block is implemented [4]. Being a critical building block in modern wireless communication systems, the PLL is used as frequency synthesizer, which is widely used to provide a stable and programmable local oscillation (LO) signal [5]. Frequency synthesizers have been developed for generating carrier frequencies covering major communication standards such as GSM, WCDMA,

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WLAN and Bluetooth. However, they require multiple VCOs, power hungry poly-phase filters or high-frequency LO buffers and dividers [6]. Conventional frequency synthesizers are implemented based on the voltage-controlled oscillator and the phase/frequency detector and charge-pump combination [7].

Despite of apparent simplicity, the traditional charge-pump PLL shows signs of breaking down when attempted in a nanoscale Complementary Metal Oxide Semiconductor (CMOS) technology, especially as part of a system-on-chip (SoC) [8]. The implementation of all digital phase locked loop (ADPLL) in frequency synthesizer has proven a reduction in the power and area eliminating the need for complex, power, and area hungry blocks such as, an analog to digital converter (ADC) or a time to digital converter (TDC) [9]. An architectural issue in these ADPLL is the absence of a quantitative value for the phase error. These results in a blind control of the Digital Control Oscillator (DCO) output frequency and may lead to loop instability [10]. However, for circuit operation at the harmonics, the requirement for the LO power is rather high. It is still a challenging task to achieve the required system specifications while maintaining reasonable power consumption in the synthesizer design [11]. An ideal frequency synthesizer generates a stable signal, which is ideally a single tone in the frequency domain. In reality, the signal is not pure, and unwanted pieces of information are added to the signal in two ways: random or deterministic signals [12]. Frequency Synthesizers are used in a wide range of RF applications. The narrow-band FM transceivers are usually used in mobile communication network *e.g.* public safety applications, which employ a huge number of channels in a limited bandwidth [13]. In such applications, it is required to have a stable LO signal with minimum phase noise, in order to avoid the channel interference [14].

Phase noise and spurious tones often limit the overall synthesizer performance. The noise from the synthesizer and the spurious tones can be reduced by narrowing the PLL bandwidth [15]. But the narrowband PLL suffers from long settling time. Consequently, there is a trade-off to determine the synthesizer performance in terms of the phase noise, the spurious tone, and the settling time [16]. Fractional-NPLLs typically use noise-shaping coarse quantizers to control their instantaneous output frequency. The resulting quantization noise is distorted by non-ideal analog components within the PLL, which induces undesirable spurious tones [17]. For the requirement of synchronization, high speed and high frequency equipment may be employed in phase-locked loop. This causes power consumption and large chip area in the circuits, which are the major concerns. Extreme high power consumption is also the disadvantage [18]. Also, the delay of the feedback path limits the speed performance of the circuit and its linear input range and can lead to average differential outputs with the wrong polarity, which disturb the acquisition process of the PLL that may reduce phase accuracy [19]. Hence, the synthesizer is required to cover all wireless standards while achieving broadband operation, the synthesizer had to comply with the demanding phase noise and spur requirements over the complete tuning range. It should be mentioned that scaled CMOS implementations typically allow for lower power dissipation [20].

In order to reduce the power consumption of VDCO, which constitute undesirable phase noise. Hence, we propose a new digital amplitude control circuit (DACC) for VDCOs, applied in the Hybrid PLL. The proposed hybrid Phase Locked Loop (PLL) consists of a phase detector that compares two input signals and produces an error signal.

The error signal is then filtered using low-pass filter to drive both Voltage Controlled Oscillator (VCO) and Voltage digitally controlled oscillator (VDCO), which creates an output phase. The output is fed back through a divider to the input of the system. Depending on the application (LTE/GSM), the output of the VCO or VDCO provides useful information for wireless application. The remainder of this paper is organized as follows: The works related to PLL frequency synthesizer is explained in Section 2. Similarly, our proposed method is explained in Section 3. In Section 4, the results and discussion is given and followed by conclusion in Section 5.

2. RELATED WORK

The background of literature related to PLL frequency synthesizer is documented below.

A. Li *et al.* [21] exhibited a mm-wave sub harmonic injection-locked (SHIL) Fractional-N frequency synthesizer for wireless multiband point-to-point backhaul communications. The SHIL synthesizer actualized a low phase noise 4.5-6.1 GHz and infused its output to a ÷3/÷4 dual-modulus divider took after by an ultra-wideband injection-locked frequency-multiplier (ILFM) chain to accomplish fabulous phase noise over an ultra-wide frequency tuning. A rippled phase response around 0° was created by ILFM over a wide frequency limit to essentially upgrade the locking range and to take out mm-wave frequency calibration loops. Fabricated in a 65 nm CMOS process, the synthesizer model measured a consistent output frequency range from 20.6 to 48.2 GHz with frequency resolution of 220 kHz and output phase noise between −107.0 and −113.9 dBc/Hz at 1 MHz while expending 148 mW and possessing $1850 \times 1130\ \mu m^2$.

L. Chen *et al.* [22] presented a direct-conversion tuner for both Very High Frequency (VHF) and Ultra High Frequency (UHF) bands. The tuner accomplished a noise figure of 2.5-3.5 dB at VHF band and 2-3 dB at UHF band. An outer band-pass filter was embraced for radio frequency pre-filtering and giving a direct current conduction way. The system-level co-design and pre-selecting filter further acquire 33 dB third-order harmonic rejection proportions without utilizing harmonic rejection mixers. A quantization-noise-compensated fractional-N frequency synthesizer was actualized, accomplishing 0.5° incorporated phase error (1 kHz to 4 MHz) at 666 MHz. The PLL infused compensation current into the loop filter during delay time, which accurately tracks the VCO output frequency. Exceptionally reconfigurable analog baseband with 0.5-4 MHz bandwidth capacity and 6-54 dB gain was coordinated. The tuner was executed in 65 nm CMOS process, involves a range of 4.2 mm^2 and expends just 72 mW from a 1.2 V voltage supply.

X. Yi *et al.* [23] developed a completely integrated 60 GHz frequency synthesizer with an in-phase injection-coupled quadrature voltage-controlled oscillator (IPIC-QVCO). Through a specific symmetrical coupling system shaped by diode-associated transistors, the in-phase coupling was acknowledged in the IPIC-QVCO, which diminishes both phase noise and phase error. A minimized inductor-less divider chain was intended to lessen power utilization and a self-revising low spur charge pump was also utilized to lessen reference spur. A standalone 60 GHz IPIC-QVCO and a fully integrated PLL are actualized in standard 65 nm low power CMOS. The estimation results demonstrated that the quadrature voltage-controlled oscillator (QVCO) covers a fre-

quency range from 57.88 to 68.33 GHz while expending 11.4 mW power from a 1.2 V supply. The phase noise of the QVCO was −92 ~ −95 dBc/Hz at 1 MHz with −178.1 ~ −179.7 dBc/Hz figure of merit. The tuning scope of the frequency synthesizer was from 57.9 to 68.3 GHz and the power consumption was 24.6 mW. The phase noise of the frequency synthesizer was −89.8 ~ −91.5 dBc/Hz at 1 MHz over the frequency band.

S. Levantino *et al.* [24] presented the multiplying delay-locked loop accomplishing fine fractional-N frequency synthesizer and established a programmed cancelation of the phase detector offset, in spite of the fact that multiplying delay-locked loops permitted clock frequency multiplication with low phase noise and jitter, their application had been so far restricted to integer-N multiplication and the accomplished reference-spur performance had regularly constrained by time offsets. Both capacities were empowered by insertion of a digital-to-time converter (DTC) in the reference way. The synthesizer, executed in a standard 65 nm CMOS process, possessed an area of 0.09 mm, and produced a frequency between1.6 and 1.9 GHz with a 190 Hz resolution from a 50 MHz quartz-based reference oscillator. In fragmentary *N* mode, the integrated root mean square jitter, including random and deterministic components, was underneath 1.4 ps at 3 mW power utilization, prompting a jitter-power figure of merit of 232 dB. In that mode, the circuit accomplished Root Mean Square jitter of 0.47ps at 2.4 mW powers and figure of merit of 243 dB.

C. Venerus and I. Galton [25] proposed the fully-integrated digital fractional-NPLL taking into accounts a second-order frequency-to-digital converter (FDC). The PLL's quantization noise was almost indistinguishable to that of a traditional analog delta-sigma modulator based PLL (ΔΣ-PLL). Consequently, the quantization noise was high pass formed and was smothered by the PLL's loop filter to the point where it was not a contributor to the PLL's output phase noise. Nonetheless, rather than ΔΣ-PLL, the PLL had an altogether digital loop filter and its simple segments were moderately unresponsive to non-ideal analog circuit conduct. In this way, it offered the execution advantages of a ΔΣ-PLL and the zone and versatility benefits. Furthermore, the PLL's oscillator consolidated a switched-capacitor frequency control element that was uncaring to supply noise and parasitic coupling. The PLL was executed in 65 nm CMOS, had a dynamic range of 0.56 mm^2, disperses 21 mW from 1.0 and 1.2 V supplies, and its deliberate phase noise at 3.5 GHz was −123, −135, and −150 dBc/Hz at offset of 1, 3 and 20 MHz, separately.

Alex Tourigny-Plante *et al.* [26] presented an open and flexible digital phase lock loop optimized for laser stabilization systems. It is based on a cheap and easily accessible FPGA-based digital electronics platform (Red Pitaya), running our open-source firmware. A PC-based software interface allowed controlling the platform and optimizing the loop parameters remotely. To demonstrate the platform's capabilities, this work implemented a fiber-noise canceler over a 400 m fiber link. Noise cancellation was achieved over a 10 kHz bandwidth, a value limited mainly by the delays introduced by the actuator and by the round-trip propagation over the fiber link and measured a total latency of 565 ns for the platform itself, limiting the theoretically achievable control bandwidth to ≈ 225 kHz.

Katarzyna Balakier [27] reviewed the advances in the development of semiconductor laser-based OPLLs and describes how improvements in performance have been enabled by improvements in photonic integration technology. This work also described, the first OPLL created using foundry fabricated photonic integrated circuits and off-the-

shelf electronic components. Stable locking has been achieved for offset frequencies between 4 and 12 GHz with a heterodyne phase noise below –100 dBc/Hz at 10 kHz offset. This has been the highest performance yet reported for a monolithically integrated OPLL and demonstrates the attractiveness of the foundry fabrication approach.

3. HYBRID PLL FREQUENCY SYNTHESIZER WITH DIGITAL AMPLITUDE CONTROL CIRCUIT

Wireless communication is the one that has huge universal wireless devices, from wireless sensors and tags to mobile terminals which requires a diverse amount of frequencies. A frequency synthesizer is an electronic system for generating any vary of frequencies from a single fastened time base or generator. For designing frequency synthesizer, Phase Locked Loop (PLL) is an essential one that generates an output signal whose phase is related to the phase of an input signal. Voltage Controlled Oscillator (VCO) is one of the most essential building blocks for PLL. A VCO's function is to generate periodic signal, whose frequency is dependent on tunable applied input voltage. For Hybrid PLL, there are two oscillators namely VCO and Voltage digitally controlled oscillator (VDCO). These oscillators require high power for producing the required signal that may affect the performance of the whole system. These power fluctuations may cause phase noise and also the phase accuracy of the system is not satisfied. Hence, the proper remedy is needed to resolve the issue of power consumption in Hybrid PLL. This motivates the need for highly accurate and low power, low phase noise frequency synthesizer that can be fully integrated together with digital circuits with standard available low-cost Complementary Metal Oxide Semiconductor (CMOS) technologies.

The proposed hybrid Phase Locked Loop (PLL) consists of a phase detector that compares two input signals and produces an error signal, which is proportional to their phase difference. The error signal is then filtered using low-pass filter. This filtered error signal is used to drive both Voltage Controlled Oscillator (VCO) and Voltage digitally controlled oscillator (VDCO), which creates an output phase. The output is fed back through a divider to the input of the system. Depending on the application (LT E/GSM), the output of the VCO or VDCO provides useful information for wireless application. But the power consumption of VDCO is quite high, which also constitute undesirable phase noise. Hence, we propose a new digital amplitude control circuit (DACC) for VDCOs, applied in the Hybrid PLL. The proposed DACC consists of VDCO core, Degeneration resistors, weighted resistors and a peak detector. Here, two versions of VDCO are presented: one has limiters while the other did not have limiters. For suppressing noise that causes small amplitude fluctuations, VDCO with limiters is used. At the same time for suppressing other noise, VDCO without limiter is used. The degeneration resistors are used to control the amplitude of the VDCO, which will control the power deviations. A set of six weighted resistors with transistor switches are used in this design to make the current adjustments. A peak detector is used to detect the amplitude of the VDCO. Our proposed method helps us to keep the VDCOs at optimum amplitude over temperature and voltage variations. The whole system is fabricated in a Complementary Metal Oxide Semiconductor (CMOS) process in order to provide reduced chip area, less spurious tone and wide tuning range. Additionally, we utilize a Lock check circuit to

provide phase accuracy and also to determine the peak-to-peak phase error from the primary phase detector. Hence, our Hybrid PLL frequency synthesizer system will provide less power consumption and reduced phase noise along with tremendous phase accuracy.

3.1 Proposed Hybrid PLL

The design of the proposed multi-standard Hybrid PLL was implemented through the division of the GSM, EDGE, and LTE bands as follows: GSM, EDGE, and low-band LTE are covered by the voltage digitally controlled oscillator (VDCO), whereas high-band LTE frequencies are generated by the VCO. The fact that both oscillators never work simultaneously allows us to share the conventional analog feedback loop of the PLL. By merging the PLL feedback loop and using digital calibrations, the Hybrid PLL achieves low power consumption characteristics while keeping its size smaller than other multi-standard PLLs. Frequency locking is carried out with the frequency-locked loop (FLL), which contains counter-based automatic frequency control (AFC) and frequency-to-digital converter (FDC) circuits, as illustrated in Fig. 3 (a). Once frequency locking is completed, phase locking is performed by the PFD/CP. Due to the strict in-band phase-noise requirements, the distortion caused by the quantization error of the TDC and the DCO in an ADPLL alone would not grant the satisfaction of the specifications mentioned in Section 2. Therefore, the main feedback loop of the proposed system was implemented using conventional CP-PLLs, which have better in-band phase-noise performance than ADPLLs. The design procedure of this system is as follows.

3.1.1 GSM/EDGE mode operation

In GSM/EDGE mode, strict requirements are put on the out of-band phase noise for the PLL. Two-point modulation is one of the most commonly used methods for PM in RF frequency. The key principle of two-point modulation consists of dividing a modulated signal into two parts and applying it to two different points in the circuit. In our PLL, GSM/EDGE phase information is contained in the phase-modulation word (PMW), which is differentiated to obtain the frequency-modulation word (FMW) and then fed into the Σ-δ modulator (SDM) and the VDCO, as shown in Fig. 1. The frequency information is therefore processed at two different points in the PLL, making the PLL behave as a wide bandwidth phase modulator. Moreover, the gain calibration of both the SDM and the oscillator is essential; hence, a feedback loop is needed in order to perform such calibration. In this system, as depicted in Fig. 1, the oscillator used in GSM/EDGE mode is a VDCO, and gain calibration is implemented with a digital feedback loop.

The VDCO is a dual control oscillator, meaning that it can be driven simultaneously by a voltage and a digital frequency control word (FCW). The gain calibration circuits were implemented in order to reduce the distortion in the gain characteristics of the VDCO and the SDM. Since the gain of the SDM is steady, its calibration can be easily performed. However, the gain of the VDCO is susceptible to process-voltage-temperature (PVT) variations and is dependent on both its frequency resolution and operating frequency. Therefore, the gain calibration of the VDCO could be regarded as a more complex process. After locking the PLL, the VDCO frequency variation is measured from the gain mismatch control (GMC), where the corresponding VDCO gain mismatch (VGM) coefficient is generated. This is then delivered to the scaler block, which nor-

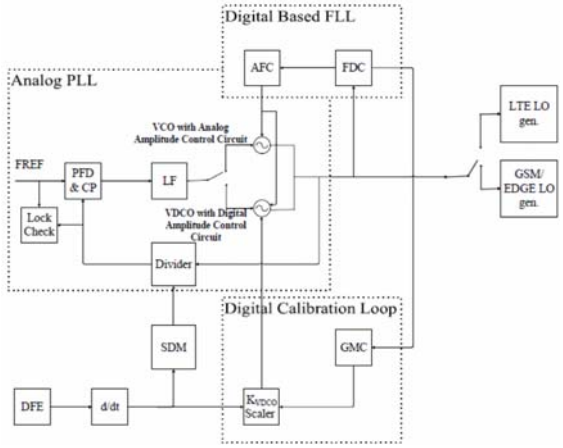

Fig. 1. Multi-standard frequency synthesizer based on the proposed hybrid PLL.

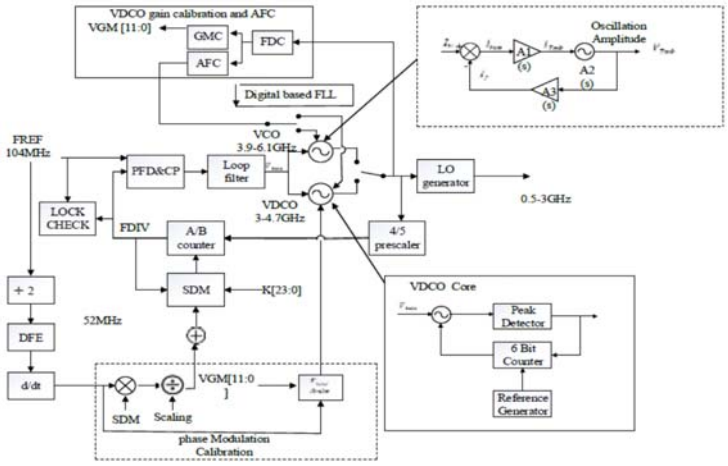

Fig. 2. Detailed block diagram of the hybrid PLL.

malizes the VDCO gain. If, by any circumstance, the gains of both the SDM and the VDCO were to have a mismatch, their desired all pass response would be lost. This may cause additional distortion. For this reason, gain calibrations must be performed before frequency modulation starts. Once the PLL locking is done by the initial frequency acquisition via the FLL, V_{CTRL} is lock around $V_{DD}/2$ improves the gain linearity of the VDCO; therefore, it can enhance the performance of the transmitter. The amplitude modulation word (AMW) is fed into the digital-to-analog converter (DAC), whose output signal passes through a low-pass filter (LPF) and into the amplitude modulation (AM)/PM combiner that also counts with a drive amplifier (DA).

3.1.2 LTE mode operation

It is difficult to tune the whole frequency range of 2-GHz of the LTE band with on-

ly one oscillator, which respects the required specifications of this standard. Hence, using of multiple oscillators is the most common implementation method to realize wide frequency tuning oscillators. The use of multiple oscillators considerably increases the chip area. However, the required specifications can be satisfied more cleverly. To fulfill the requirements of LTE, the phase-noise specifications are considered to be more important than keeping the size small. Therefore, the proposed PLL divides the whole LTE band into a low band and a high band; each of them, respectively, covered by an independent oscillator. To further lower the in-band phase noise, three main approaches were considered. These are the reduction of the CP current mismatch, a high-order SDM with fast operation, and a low VCO gain. The reduction of the CP current mismatch was realized through a dual compensation topology. This topology flattens the up/down current variation curves by using two operational amplifiers. The SDM improves the in-band phase-noise performance of the PLL through noise shaping. As the SDM's order increases, its noise-shaping characteristic is enhanced, which reduces the in-band phase noise more effectively. Nevertheless, high-order SDM's inherent circuit complexity has to be considered. Taking into accounts this tradeoff, the proposed architecture adopts a third-order multi-stage noise shaping (MASH) type SDM. The gains of the two oscillators adopted in the proposed system, both remain at a level lower than 100 MHz/V for all frequency bands. For a desired oscillation frequency, constant voltage sensitivity is obtained by adopting the AFC technique, which forces the oscillators to operate at the center of their transfer curve. Low VCO gain and constant voltage sensitivity both contribute to the enhancement of the PLL's stability and phase-noise performances. This paper's frequency synthesizer architecture is based on a conventional CP type II fractional-PLL. The PLL's loop bandwidth was set to 200 kHz to obtain a low LO rms jitter. Use of a tunable loop filter guarantees the phase margin of the PLL to be always higher than 45 for all frequency bands.

3.1.3 Lock check

The reference clock counter (RCC) and the feedback clock counter (FCC) are N bit binary counters. The comparator compares the values of both counters. The Timer is an M bit counter. The PLL lock flip flop remembers the output worth of the detector, indicating if the system (the PLL) is in lock state or not. The operation is predicated on the comparison of equality of frequencies of reference and feedback signals. Initial the RCC, FCC, Timer and the PLL lock flip flop are reset. Then the RCC and FCC counter begin to count severally from one another. Once the RCC gets its maximum value, the RCC and FCC counters are compared. If these counters are equal, an enable signal (EN) is made on the output of the comparator that permits the Timer to count whereas the EN is active (logical "1"), the Timer continues to count till it gets to its maximum value. Subsequently, a logical "1" is about in PLL lock flip flop, which shows that the PLL is in lock condition. Once the PLL is in lock (when a logical "1" is in PLL lock flip flop), and therefore, the values of RCC and FCC become an on-equal, the EN signal switches to "0", the Timer resets, and whereas the EN is adequate to "0", the Timer counts to fix the time, within which the PLL comes out from lock condition. Once the Timer counts up to some outlined value, a "0" is about in PLL lock flip flop. It means that the PLL is in unlocking condition.

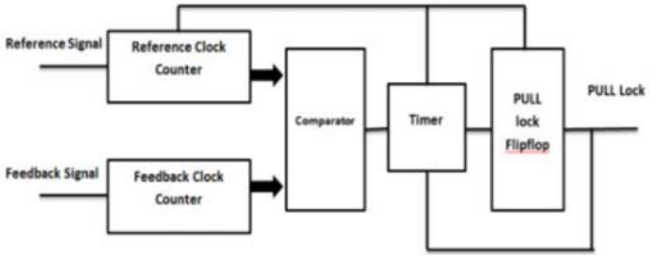

Fig. 3. Block diagram of the lock check.

3.2 Circuit Implementation

3.2.1 VDCO with digital control loop

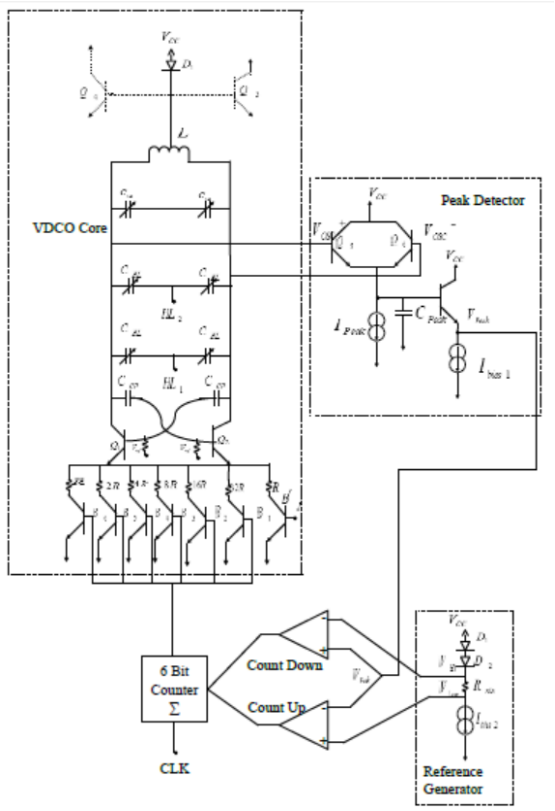

Fig. 4. VDCO topology with adjustable degeneration resistors placed in a digital automatic-amplitude control loop.

4. RESULTS AND DISCUSSION

This section shows the proposed ECG signal analysis mainly the QRS complex de-

tection and the results obtained by them.

System configuration:
Operating System: Windows 8
Processor: Intel Core i3-6300
Processor Base frequency: 3.80 GHz
Cache: 4 MB Smart cache
Processor graphics: 3.80 GHz
RAM: 4 GB
Platform: Cadence
Dataset: Physio Net MIT-BIH traces.

Here, the ECG signals are sampled at rate of 360 samples with 11-bit resolution. All the traces of database are usable and some are very noisy due to heavy artifacts probably due to the disconnection of the sensing devices. The databases are considered from the ANSI/AAMI EC13 Test Waveforms.

4.1 Experimental Results

The above figure shows the response of the fourth order filter in terms of frequency and gain. From the simulation result, it is clear that the phase margin of our proposed filter yields –45° for the frequency range from 10 to 1000 k rad/sec.

Fig. 8 shows the phase-noise measurements for both LTE and GSM modes. The resulting phase noise in the GSM mode has more mismatches. A possible cause of the mismatch between simulation and measurement is the parasitic capacitance linked to the common source node of the cross-coupled pairs in both oscillators.

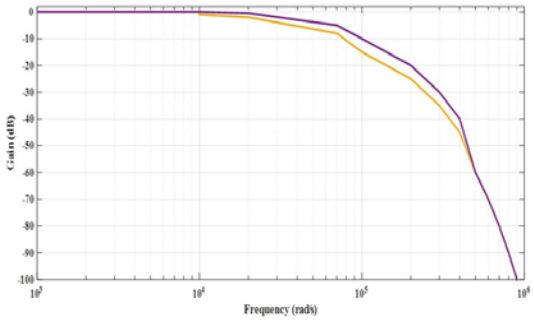

Fig. 7. AC response of the fourth-order loop filter.

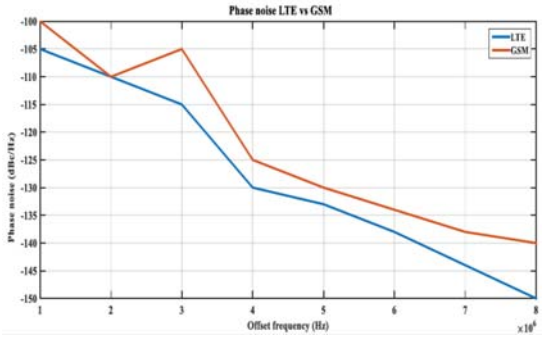

Fig. 8. LTE mode phase noise and GSM mode phase noise.

The measured output spectrum of the proposed system is shown in Fig. 9; the spectral density of GSM and EDGE modes at a 400-kHz offset is 64.7 and 57.7 dBc, respectively. These performances are obtained to get the low level phase noise of the PLL at that offset. In addition, the average phase error of the transmitter's modulated output in the GSM mode is 0.79.

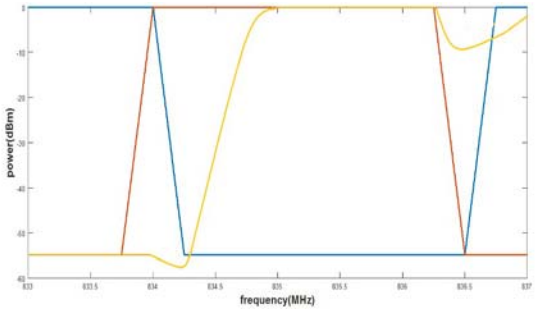

Fig. 9. Power of frequency synthesizer.

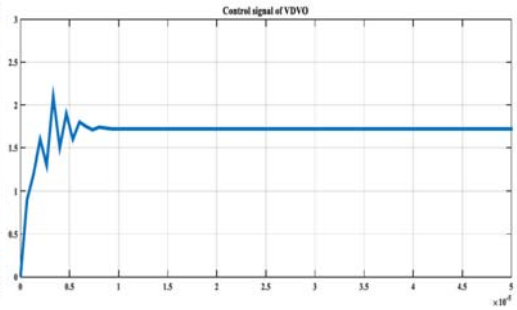

Fig. 10. Control signal of VDCO.

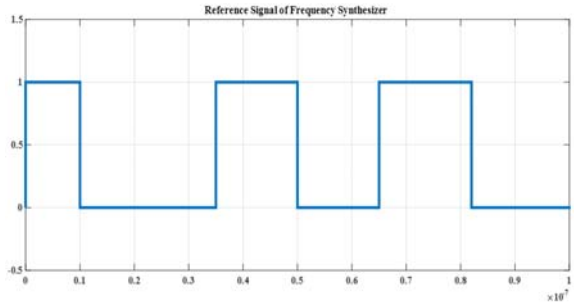

Fig. 11. Reference signal of frequency synthesizer.

Fig. 11 shows the control signal and reference signal, which is a square pulse of frequency 30 MHz. This reference signal is given to the PFD. The VDCO block uses control signals to maintain the frequency of the synthesized signal. This signal initially fluctuates for about 10 microseconds, but then stabilizes to a constant value of 7/4. This occurs when the model reaches a steady state, that is, when the frequency of the synthesized signal is close to 100 MHz.

4.2 Performance Evaluation

Some criteria were employed in accordance to the recommendations to assess performance of frequency synthesizer such as Figure of Merit (FoM), phase noise, spur, lock time.

4.2.1 Figure of merit

The figure-of-merit (FoM) of a PLL which can characterize frequency synthesizer in terms of its rms jitter and its power consumption is defined as follows:

$$FOM_{PLL} = 10\log\left[\left(\frac{\sigma_t^2}{1\sec}\right)\left(\frac{Power}{imW}\right)\right]. \tag{1}$$

Where σ_t- rms jitter. The unit of FOM_{PLL} is decibels. A smaller FOM_{PLL} corresponds to a better PLL design.

4.2.2 Phase noise

The total phase noise in conventional method is given by the sum of phase noise at PFD, VDCO and divider. The total phase noise is given by the Leesons equation. The first part of equation that is $f_0/2Q_Lf_m$ gives the phase noise due to VDCO. The second part of equation that is FKT/P_s gives the phase noise due to loop filter. The third part of the equation that is $f_c/f_m + 1$ gives the phase noise due to the PFD. The Leesons equation gives is as follows:

$$PhaseNoise = 10\log_{10}[1/2((f_0/2Q_Lf_m)^2 + 1)(FKT/P_s)(f_0/f_m + 1)] \tag{2}$$

where f_m is offset frequency, f_0 is free running frequency of VDCO, Q is the quality factor, F is the noise figure, k is the Boltzman constant, T is temperature.

4.2.3 Spur

The spurs are caused by non-idealities within the PLL element like mismatched propagation delay within the PFD and CP, charge injection and current mismatches within the CP. thus modeling of spurs is needed.

$$Spur\ in\ dB = 20.\log_{10}\left(\frac{KVDCO - vn}{2 - fn}\right) \tag{3}$$

where, vn is the peak voltage measured at the fn, KVDCO is the gain of VDCO.

4.2.4 Lock time

Lock time should be less for a better frequency synthesizer. The lock time is effected with the change in bandwidth.

$$Lt = (400/Fc)(1 - \log_{10}\Delta F) \tag{4}$$

Where, Lt is lock time in microseconds and Fc is the loop bandwidth in KHz. ΔF is the ratio of frequency tolerance to frequency jump.

4.3 Comparisons

The Frequency Synthesizers may be analyzed and processed using several techniques such as single standard, multi standard *etc.* In such techniques the frequency division is done with the help of fractional N classifiers and digital PLL that uses the figure of merit as a performance parameter.

Table 1. FoM comparison of existing with proposed method.

Power consumption (mW)	Jitter (ps^2)		
	Digital Intensive PLL	Digital ΔΣ Fractional *N* PLL	Proposed
1	10	100	1
10	1	10	0.1
100	0.1	1	1

Our proposed method uses a Hybrid PLL to detect the phase from the reference signal. The FoM comparison between our proposed methods with existing techniques is shown in Table 1. From table, it is evident that our proposed frequency synthesizer produces better jitter with greater figure of merit than the existing PLL. The below figures show the comparison graph between the proposed system with the other existing classifiers such as, Digital Intensive PLL and Digital ΔΣ Fractional N PLL.

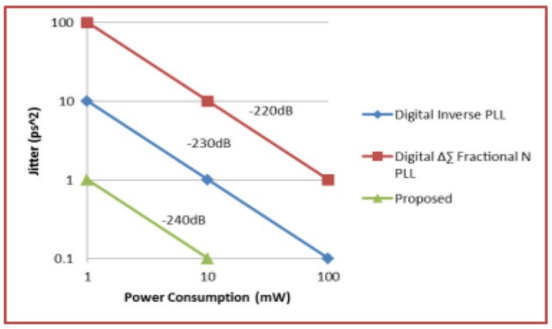

Fig. 12. FoM comparison of different frequency synthesizer.

The FoM of the proposed PLL is −239 dB, comparable to that of existing single-standard PLLs. Furthermore, when compared to other multi-standard PLLs, the proposed PLL shows a superior FoM and smaller size.

Table 2. Comparison of existing with the proposed method.

Parameter	Analog PLL	ADPLL	Proposed
Phase Noise (dBc/Hz)	−104	−106	−110
Spur (dBc)	−48	−55	−31.47
Lock time (μs)	0.175–1.2	0.1–0.175	0.75–0.1

The values obtained from the cadence simulation are shown in the Table 2. The comparison for the parameters phase noise, spur and lock time is done among below for analog PLL, ADPLL and the proposed system.

The uncertainty of a synthesizer's output is characterized by its phase noise (or spur level) at a precise frequency offset from the required carrier frequency in unit of dBc/Hz (or dBc). The unit of dBc/Hz measures the quantitative relation (in dB) of the phase noise power in 1Hz bandwidth at a precise frequency offset to the carrier power. The

entire parameters mentioned in the proposed method are compared with the help of existing frequency synthesizers.

The phase noise measured in dBc/Hz ranges from −110 dBc/Hz, which mean that the phase noise decreases. Electrical components in PLL building blocks generate noise. This noise affects the PLL, creating phase variations of the PLL output signal, so called phase noise. Phase noise affects both the transmitted and received signal, and will distort the modulation of transmitted data. But from the results, we can know that our system have low effect on received and transmitted signal since the phase noise is lower.

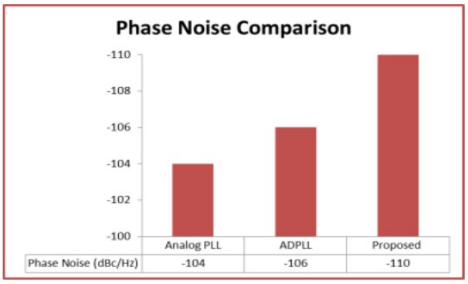

Fig. 13. Phase noise comparison of different frequency synthesizer.

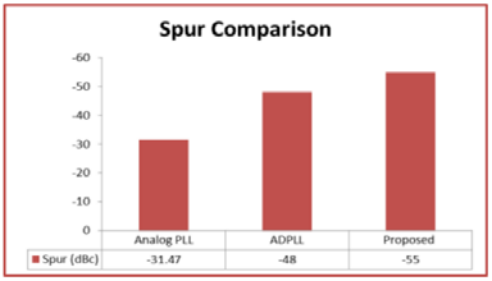

Fig. 14. Spur comparison of different frequency synthesizer.

Similarly, the unit of dBc measures the ratio (in dB) of the spur (also known as tone) power at a certain frequency offset to the carrier power. The phase noise requirement of a frequency synthesizer depends on applications. A small fraction of the reference clock will always leak through the loop-filter and modulate the VCO, creating side bands around the oscillator output at a distance equal to the reference frequency. When the PLL frequency change, the reference spurs will move along with the carrier.

The spur measured in dBc/Hz ranges from −31.47dBc, which mean that the spur value is lower than the existing systems.

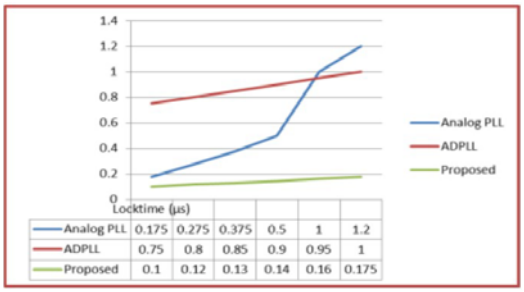

Fig. 15. Lock time comparison of different frequency synthesizer.

The lock time measured in microseconds 0.175 µs to 0.1 µs, which mean that the lock time is very low and hence, the speed is higher. From the results, it is clear that our proposed system will generate a superior phase noise, better locking speed, reduced sour and good figure of merit and hence, our system will give minimum power consumption.

4.4 Discussions

The performance summary of the synthesizer and compares it with some other synthesizers in the existing system is analyzed. In our design, we have focused on achieving low power consumption and a low phase noise. Wide tuning range is achieved, since the circuit is intended for the application of GSM, LTE applications. Our design might also be useful for other applications such as EDGE. Here, power consumption is crucial, and a wide tuning range, a low VCO phase noise and good radiation hardness are mandatory. In this context, the low flicker noise of VDCO is helpful to achieve a low phase noise at small frequency offsets than the existing frameworks. Together with the CMOS logic offers the opportunity to design low-noise, wideband PLLs for flexible applications. The value of locking time is much lower than the existing and hence, the locking speed is improved.

5. CONCLUSION

A multi-standard frequency synthesizer, based on the novel Hybrid PLL architecture has been presented in this paper. By using a digital calibration loop and a VDCO, the proposed PLL achieves good phase resolution and jitter characteristics for GSM/ EDGE and LTE standards. The proposed chip, implemented in a 65-nm CMOS process, occupies 0.72 mm and consumes 26.4 mW. In practice, the designed Hybrid PLL successfully satisfies the in-band and the out-of-band phase-noise specifications required by GSM/EDGE and LTE standards. Therefore, the suggested multi-standard frequency synthesizer is competitive for use in commercial multi-standard applications. This paper has presented VCOs with both analog and digital automatic-amplitude control loops. A best phase noise of 108.5 dBc/Hz at 100-kHz offset was achieved with the digital loop in a low-gain mode. The VCOs had a very wide tuning range. The phase noise was almost constant over a temperature range of 50oC to100oC. The design of the feedback digital amplitude control circuit that helps to achieve this performance has been discussed.

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