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Multi-Scan Architecture with Scan Chain Disabling Technique for Capture Power Reduction

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High test power dissipation can severely affect the chip yield and hence the final cost of the product. This makes it of utmost important to develop low power scan test methodologies. In this work we have proposed a capture power minimization method to disable those scan chains, needless for the target fault detection, during the capture cycle for multi-scan testing. This method combines the scan chain clustering algorithm with the scan chain disabling technique to disable partial scan chains during the capture cycles while keeping the fault coverage unchanged. This method does not induce the capture violation problem nor does it increase the routing overhead. Experimental results for the large ISCAS'89 benchmark circuits show that this method can reduce the capture power by 43.97% averagely.

***Keywords*:** capture power, low power testing, power consumption, scan-based testing, scan chain

1. INTRODUCTION

Excessive power consumption during scan-based testing has been a strict challenge for VLSI design. Essentially, a circuit consumes more power in test mode than in normal mode [1]. In the shift cycle, a test vector is scanned into the scan chain, simultaneously with the scanning-out of the previous test response. In the capture cycle, the test vector loaded into the scan chain during the shift cycle is applied to the combinational part of the circuit and the response of the circuit is captured into the scan chain. For scan-based testing, when capturing responses, typically a much larger percentage of flip-flops will change values. What's further, the change in the flip-flops will cause other gates in the combinational part of the circuit to switch. The rippling effect of switching activity can cause test power to be significantly high. The induced heat dissipation may not only cause logical error in a fault-free chip leading to an unnecessary loss of yield, it can even destroy the chip under test [2, 3].

Disabling partial scan chains during testing for minimizing unnecessary power consumption is a popular technique which has been implemented in many research works, such as [6, 8]. Obviously, the more scan chains turned off in the capture cycle can lead to more power savings. Therefore, it is critical to recognize the observing scan cells for the desired fault effects and then properly cluster them into scan chains as dense as

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possible. In this paper, we combine techniques of scan chain clustering with scan chain disabling to maximize the number of disabled scan chains in the capture cycle. Experimental results show that the proposed method can achieve an average capture power reduction by 43.97%. The rest of this paper is organized as follows. Section 2 reviews some related works. Section 3 presents the details of the proposed method. Section 4 reports the experimental results on the large ISCAS'89 benchmark circuits. Section 5 concludes this paper.

2. RELATED WORK

Several techniques have been proposed for reducing test power exploiting the scan chain architecture [5-8]. In [6] the authors proposed a dynamic partitioning approach which can adapt to the transition distribution of any test pattern and can deliver significant peak power reduction. In [7], the unused scan chains are switched off to minimize the test power for larger designs. The method in [8] divides scan cells into some groups by using cell type classification to avoid formation of conflict cases. Then, based on the divided groups, X-bits are filled to reduce the capture power during scan-based testing. The authors in [9] proposed to reduce dynamic power consumption in scan chain by introducing XOR gate at selected places in the traditional scan chain showing that switching activity can possibly be reduced within modified scan architecture. Many methods have been proposed to reduce test power during the shift cycle [10-12]. The method in [10] adds additional circuitry to the scan cells to hold the outputs at a constant value during scan. This method substantially reduces the shift power. However, it introduces undesired delay leading to performance degradation. The technique based on scan cell reordering for power minimization in full scan sequential circuits was proposed in [11] where techniques of random ordering and simulated annealing are employed to determine the scan cell order in a given scan chain. However, the high computation complexity limits its applicability. The authors in [12] apply the control pattern to the circuit primary inputs aiming at minimizing the switching activity in the combinational part of the circuit. However, circuits are mostly controlled by scan chains rather than by the primary inputs. Therefore, the reduction in test power is restricted. The work in [13] proposes a modified scan flip-flop design which uses a dynamic slave latch to shift the test vectors and allows the static slave latch to retain the responses from the previous test vector. Through bypassing the slave latch during loading/unloading operation, the proposed flip-flop design eliminates redundant switching activity in combinational logic and hence minimizes test power. The paper in [14] proposes a logic cluster controllability scan chain stitching methodology to achieve low-power testing. The scan chain stitching is made power aware by placing flip-flops with higher test combination requirements at the beginning of scan chains, while flip-flops with lower test combination requirements are put toward the end of scan chains. This method helps in consolidating care bits toward the beginning of scan chains. Hence, a significantly lower shift-in transition is achieved in the test patterns.

As mentioned previously, during the capture cycle, all scan cells capture at the same time inducing a wide range of transitivity activity in the combinational block. Therefore, the peak power consumption is most likely to occur during the capture cycle. Reducing redundant power in the capture cycle is a critical issue for circuit testing. Many tech-

niques have been proposed to reduce the excessive capture power. Most of them split the scan chain into multiple partitions and have only one of them active during each capture cycle. Although very effective, these methods may introduce the data dependency problem when multiple scan chains capture responses at different cycles. To solve this problem, the authors in [15] proposed a method by dividing the CUT into a number of strongly connected components. Some blocking circuits are inserted to the selected scan cells. Although it can eliminate the data dependency problem, this method increases area overhead. Besides, the blocking circuits added to the selected scan cells may degrade the circuit performance. The authors in [16] employed multiple capture orders to deal with the data dependency problem. No area overhead is required for this method, but too many extra captures are executed. The paper in [17] presents a scalable approach called "Preferred Fill" to reduce average and peak power dissipation during capture cycles of launch off capture delay fault tests. This scheme in [18], called Quick-and-Cool X-fill (QC-Fill), properly utilizes the don't-care bits in test vectors to simultaneously reduce both test time and test power. The method in [19] partitions the original scan chain into several scan paths and activates these scan paths using different enable lines. Only one scan path is activated at each time to restrict the scan rippling. *S*ince the whole scan chain will be activated when the response data are captured, peak power reduction may not be guaranteed. In [20], the authors propose an automatic test pattern generation scheme for low power launch-off-capture transition test. Two techniques are explored. A bidirectional X-filling in which both line justification and logic simulation are used to reduce capture power while feeding the first test pattern into CUT. For vectors producing very large capture power, a test vector replacement scheme is applied to efficiently reduce the peak capture power. The proposed method does not change the test architecture, and thus no hardware overhead is required. Paper [21] presents a multiple capture approach to reducing the peak power as well as average power consumption during testing. This method is to divide a scan chain into two sub-scan chains, and only one sub-scan chain will be enabled at a time during the scan shift or capture operations. To deal with the capture violation problem, a pattern insertion technique is used during the capture cycle. This technique is simple and efficient to reduce capture power, however; inserting redundancy patterns to deal with capture violation problem makes the testing time longer.

3. PROPOSED METHOD

Typically, automatic test pattern generation (ATPG) proceeds in a one-fault-one-cube manner. In each generated test cube, only some circuit inputs are specified for sensitizing the target fault in the circuit under test. Depending on the circuit geometry, the activated fault effect is propagated to one or more than one circuit outputs for a later observation. A fault is thus believed to be detected by a test vector if the response is different with the correct one. However, observing the fault effect from only one circuit output is sufficient. For multi-scan testing, only the scan chain that captures the desired fault effect is essentially important to the fault detection. Enabling additional more scan chains than required is not necessary and will consume additional power. Therefore, deactivating the unnecessary capture operation by scan chains can save the capture power without affecting the fault coverage. The amount of capture power savings is proportional to the amount of disabled scan chains.

The proposed scan chain disabling method is described as follows. In the first step, test vectors are analyzed for a given test set by conducting a series of fault simulations to investigate the detection efficiency by each test vector through a further examination of each don't care bit. The employed observing scan cells are also identified. In the second step, a weighted observability graph is constructed to explore the correlation of the observing scan cells so as to assist in the later scan chain clustering process. The closely-correlated observing scan cells are expected to be clustered in a scan chain. With the clustered observability-aware scan chains, in the third step, the capture-power-aware scan chain disabling architecture is thus constructed. We give the details as follows.

3.1 Test Vector Analyses

Typically, a test cube is generated for detecting some target fault by the ATPG. Those don't care can be well examined and specified to detect additional more faults in the circuit under test. Fig. 1 shows the smallest ISCAS'89 benchmark circuit, the stuck-at-0 fault on circuit line m can be detected through sensitizing the circuit path *m* to *I* by applying test vector $V(A, B, C, D, E, F, G) = (0, X, X, X, 1, X, X)$. The activated fault effect can then be propagated to the circuit output and finally captured into the scan cells. Generally, observing the fault effect by only one scan cell is sufficient for detecting a target fault. We thus have S_0 as the observing scan cell for *V*. To improve the detection efficiency by *V*, those *X*′s can be flexibly specified as "0" or "1" to further increase the number of detected faults. As can be seen, the stuck-at-1 fault on the other circuit line *n* can be sensitized by $V'(A, B, C, D, E, F, G) = (0, X, X, 1, 1, X, X)$ through specifying the third *X* in *V* as "1". The associated fault effect can consequently be captured and observed by scan cell S_2.

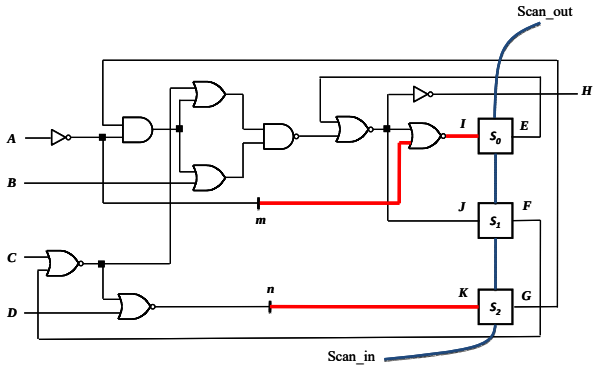


Fig. 1. An example with benchmark circuit s27.

Table 1 shows the test vector information for circuit s208. The left main column gives the original test vectors (V_1~V_{11}). The right main column presents the test vectors (V'_1~ V'_{11}) after "*X*" specifications and the employed observing scan cells. As shown, after specifications for "*X*s", the amount of detected faults by each test vector grows. For example, a total of 87 faults can be detected by test vector V'_1 after specifying the left-most "*X*" by "1" and the employed observing scan cells are Y_1, Y_2, Y_3, Y_5, Y_6, Y_7, and Y_8 respectively. Conversely, the capture operation by scan cell Y_4 is redundant and can be skipped under the same fault coverage. Similarly, the capture operations by scan cells Y_1,

Y_2, Y_3, Y_4, and Y_7 are not necessary for test vector V'_2, which can be disabled during the capture cycle.

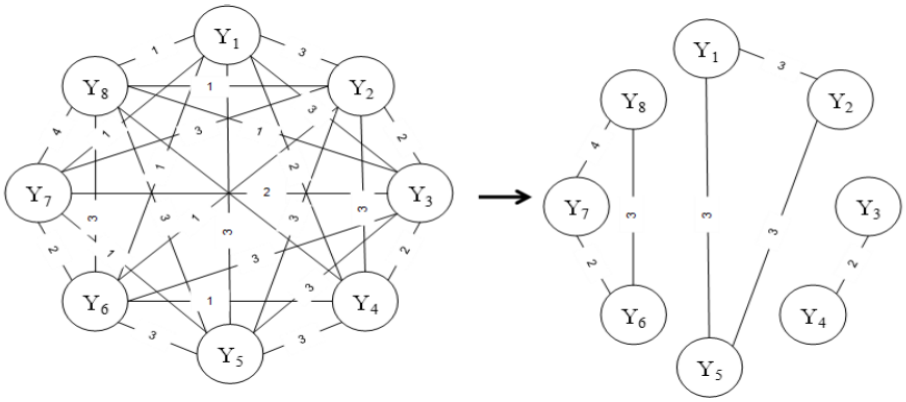
Table 1. Test vectors for circuit s208 before and after *X* specifications.

s208				
Before *x* specifications		After *x* specifications		
Test vectors	Observing SCs	Test vectors	No. of detected faults	Observing SCs
V_1 = X0xxxxxxxxx11110111	Y_8	V'_1 = 10xxxxxxxxx11110111	87	Y_1, Y_2, Y_3, Y_5,Y_6, Y_7, Y_8
V_2 = xxxxxxxxxxxxxxx0110	Y_8	V'_2 = x0xxxxxxxxx11110110	72	Y_5, Y_6, Y_8
V_3 = x0xxxxxxxxx1111xx01	Y_6	V'_3 = x0xxxxxxxxx11110001	69	Y_6, Y_7, Y_8
V_4 = xxxxxxxxxxxxxxxxx00	Y_6	V'_4 = 10xxxxxxxxx01110100	73	Y_4, Y_5, Y_6, Y_8
V_5 = xxxxxxxxxxx0110xxxx	Y_4	V'_5 = 10xxxxxxxxx0110xxxx	58	Y_1, Y_2, Y_4
V_6 = 10xxxxxxxxxxx01xxxx	Y_2	V'_6 = 10xxxxxxxxx1001xxx0	61	Y_2, Y_3, Y_4, Y_5
V_7 = xxxxxxxxxxxxx00xxxx	Y_2	V'_7 = 11xxxxxxxxx0000xxx0	41	Y_1, Y_2, Y_4, Y_5
V_8 = x0xxxxxxxxx1111x011	Y_7	V'_8 = x0xxxxxxxxx11111011	75	Y_7, Y_8
V_9 = x0xxxxxxxxx1111x10x	Y_7	V'_9 = x0xxxxxxxxx11110101	72	Y_7, Y_8
V_{10} = 10xxxxxxxxxx10xxxxx	Y_3	V'_{10} = 10xxxxxxxxx0101xxxx	58	Y_3, Y_4
V_{11} = 00xxxxxxxxxxx0xxxx	Y_1	V'_{11} = 00xxxxxxxxx1100xxx0	65	Y_1, Y_5

3.2 Scan Chain Clustering

As previously stated, the observing scan cells Y_5, Y_6, and Y_8 for test vector V'_2 are expected to be densely clustered into as fewer scan chains so that more unnecessary scan chains can be disabled to eliminate the excessive capture power. This concept is straightforward and easy to implement if test application with only one test vector is considered. However, this problem becomes fairly complicated when all the test vectors in a given test set are simultaneously put into consideration, which belongs to an NP-complete problem. To solve it, we transfer the maximum weight clique algorithm in [20] to the maximal-clique partitioning solving algorithm to deal with the scan cell clustering problem. Given an undirected graph $G = (V, E)$ where each vertex in $V = \{S_1, S_2, ..., S_n\}$ respectively represents a scan cell. The edge e_{ij} connects adjacent vertexes S_i and S_j where $E = \{e_{ij} | 1 \le i \le n, 1 \le j \le n\}$. The edge weight w_{ij} represents the number of test vectors employing the same observing scan cells S_i and S_j. For example, the edge weight $W_{12} = 3$ represents that there are three test vectors employing both S_1 and S_2 to observe the desired fault effects. A higher edge weight implies a higher expectation for these two scan cells to be clustered together in the same scan chain with regard to the capture power reduction efficiency. Fig. 2 (a) shows the weighted observability graph for circuit s208, where 8 vertexes are considered. The scan chain clustering was conducted by first partitioning the weighted observability graph into the minimal number of maximum cliques. Next, the clique with the highest total edge weight will be removed and the correspond-

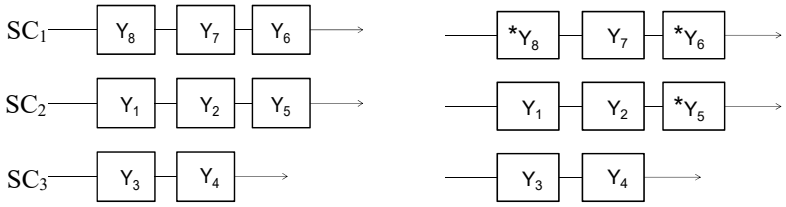
ing scan cells will be assigned into the same scan chain. This procedure will proceed iteratively until all the scan chains are fully filled. Fig. 2 (b) presents the resulting three cliques after conducting the clique partitioning algorithm.



(a) (b)

Fig. 2. (a) Weighted observability graph for s208; (b) Three cliques after partitioning.

The resulted three scan chains are presented in Fig. 3 (a). Fig. 3 (b) shows the observing scan cell distribution (marked with "*") in scan chains for V_2, *i.e.*, Y_8 and Y_6 in scan chain 1 and Y_5 in scan chain 2. As can be seen, since scan chain 3 does not contain any observing scan cell, it can be disabled during the capture cycle. Table 2 lists the enabling scan chains (marked with "∨") by each test vector during the capture cycle. Column "Cell off" gives the ratio of disabled scan cells over the total number of scan cells for each test vector.



(a) (b)

Fig. 3. (a) The scan chain architecture for s208; (b) The observing scan cell distribution for V_2.

Table 2. Scan chain enable/disable for circuit s208.

Test vectors	SC_1	SC_2	SC_3	Cell off (%)	Test vectors	SC_1	SC_2	SC_3	Cell off (%)
V_1	∨	∨	∨	0	V_7		∨	∨	37.5
V_2	∨	∨		25	V_8	∨			62.5
V_3	∨			62.5	V_9	∨			62.5
V_4	∨	∨		25	V_{10}		∨	∨	37.5
V_5		∨	∨	37.5	V_{11}		∨	∨	37.5
V_6		∨	∨	37.5					

3.3 Multi-Scan Architecture with Scan Chain Disabling Technique

We implement the proposed scan chain disabling technique adopting the clock gating scheme by which individual scan chains can be selectively enabled/disabled through outputs of the corresponding AND gates. Fig. 4 shows the multi-scan architecture. Control signal S/C decides the scan operation to be in the shift mode or capture mode. Test data is serially scanned in and broadcast to all scan chains. Signals (En_1~En_n) are sent from the decoder to respectively decide the enable/disable of individual scan chains through the clock gating scheme adopting AND gates. When En = 1, the corresponding scan chain will be enabled to either receive the input test data or capture response. When En = 0, the corresponding scan chain will be disabled. The decoder is simple and circuit-independent. The decoder complexity depends only on the number of scan chains. The induced hardware overhead is low. The required design effort including the control signal is also limited.

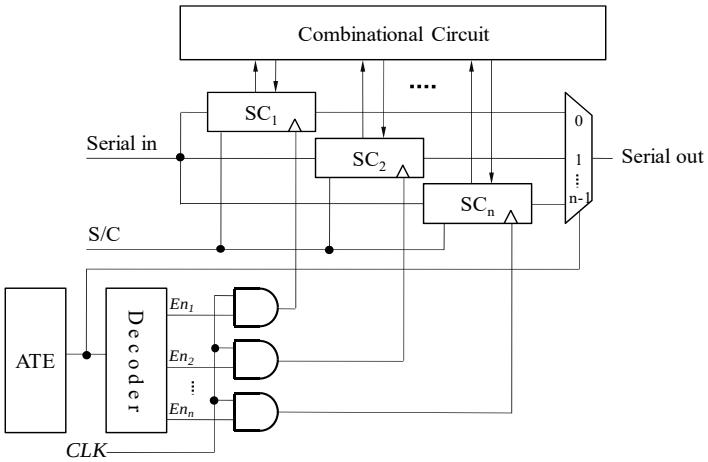


Fig. 4. Multi-scan architecture with scan chain disabling scheme.

4. EXPERIMENTAL RESULTS

We conducted experiments in C++ language on an Intel(R) Core(TM) 2 Duo CPU E4500 2.2GHz 2.5GB PC. Test sets for the large ISCAS'89 full-scan benchmark circuits are generated by the Synopsys ATPG tool "TetraMax". Power consumption is estimated by the node transition counts (NTC) between the pseudo primary input (PPI) and the pseudo primary output (PPO). Table 3 presents the experimental results. Column "Ckts" and "N_f" show the circuit name and the total number of flip-flops in the circuit respectively. Column "N_v" compares the number of test vectors before (Orig.) and after test vector compaction (Comp.). The column "Transition counts" reports the transition counts by the proposed method under the scan chain number (N_c) 4, 8, 16, and 32 respectively. Sub-column "R_T (%)" reports the transition reduction ratio compared with the traditional single scan chain scheme, which can be computed as R_T (%) = ((A – B) / A) × 100%. The last column gives the run time for each case. As can be seen from the experimental

Table 3. Experimental results for the large ISCAS'89 benchmarks.

Ckts	N_f	N_v		Transition counts				Run Time (sec.)
		Orig.	Comp.	Single-scan Method (A)	N_c	Proposed Method (B)	R_T(%)	
s1423	74	1489	75	24800	4	19960	19.5	0.6
					8	17899	27.8	0.6
					16	16901	31.8	0.6
					32	15054	**39.3**	0.6
s5378	179	5919	132	226276	4	109393	51.7	2.1
					8	94252	58.3	2.1
					16	77823	65.6	2.2
					32	73426	**67.6**	2.4
s9234	211	11056	248	587506	4	466709	20.6	57.5
					8	422226	28.1	57.6
					16	386940	34.1	57.9
					32	333100	**43.3**	58.4
s13207	638	17189	149	419006	4	240251	42.7	12.0
					8	195613	53.3	12.1
					16	169345	**59.6**	12.5
					32	183789	56.1	14.4
s15850	534	20494	238	503118	4	401964	20.1	21.4
					8	377544	25.0	21.6
					16	339114	32.6	22.2
					32	312402	**37.9**	24.4
s35932	1728	32808	44	509357	4	488316	4.1	114.0
					8	478765	6.0	114.5
					16	460940	9.5	117.2
					32	454396	**10.8**	130.89
s38417	1636	47514	226	2219851	4	1711245	22.9	139.0
					8	1460283	34.2	139.3
					16	1230805	44.6	141.3
					32	1117248	**49.7**	150.33
s38584	1426	39608	166	1033265	4	735044	28.9	85.8
					8	671325	35.0	86.1
					16	606686	41.3	87.2
					32	546312	**47.1**	94.2

results, since a bigger scan chain number gives a larger space for improving the effectiveness of scan chain clustering and hence increasing the total number of disabled scan chains during the capture cycle. The capture power reduction in transition counts grows as the number of scan chains increases in almost all cases. In the last column, we report the run time in seconds. In Table 4, we compare the transition count reduction with other methods. Results show that our method can achieve better results in most cases except the s35932 circuit. Since s35932 employs only 44 test vectors, no strong correlation can

be found among scan cells to help densely cluster the observing scan cells. Consequently, this method can achieve 43.97% of capture power reduction averagely.

Table 4. Comparisons with other methods in capture power reduction.

Circuits	Transition counts		(%) Improvement			
	Single-scan Method (A)	Proposed Method (B)	Proposed Method	Method [13]	Multiple Capture [21]	LCP-fill [18]
s1423	24800	15054	39.30	39.16	41.47	34.09
s5378	226276	73426	67.55	40.37	35.44	31.03
s9234	587506	466709	43.30	39.43	42.78	10.49
s13207	419006	183789	56.14	28.10	31.06	50.20
s15850	503118	312402	37.91	40.70	42.04	37.11
s35932	509357	454396	10.79	42.50	45.20	29.06
s38417	2219851	1117248	49.67	38.36	43.20	17.20
s38584	1033265	546312	47.13	33.54	37.40	22.03
Avg.			43.97	37.77	39.83	37.12

5. CONCLUSIONS

We have presented an efficient scan chain disabling method to reduce the capture power for multi-scan testing. In order to maximize the number of disabled scan chains, a maximal-clique partitioning algorithm is implemented to help densely cluster the observing scan cells. Scan cell clustering can be implemented by the design tool and would not introduce hardware overhead. Experimental results for the large ISCAS'89 benchmark circuits have demonstrated that this method is outstanding over similar works.

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